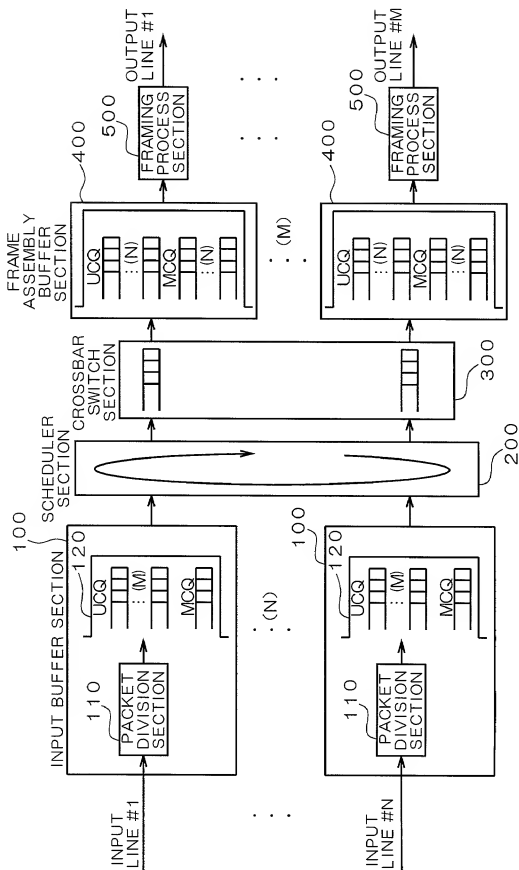


FIG. 1



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FIG. 3

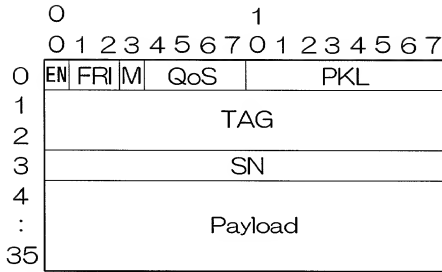


FIG. 3

FIG. 4

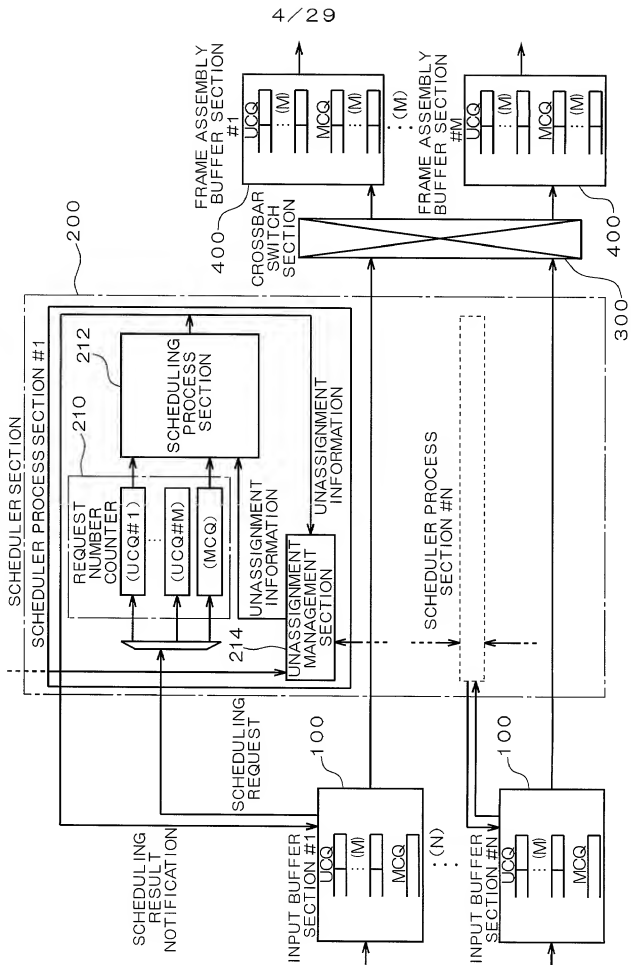
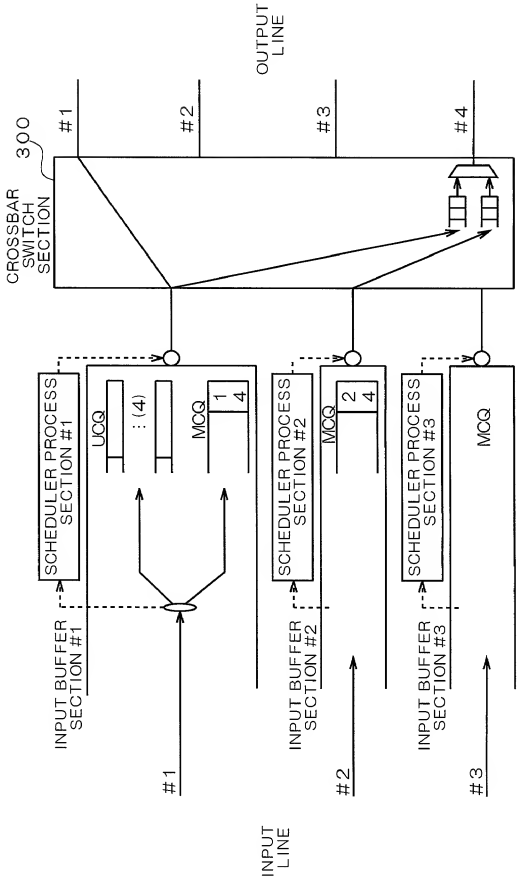
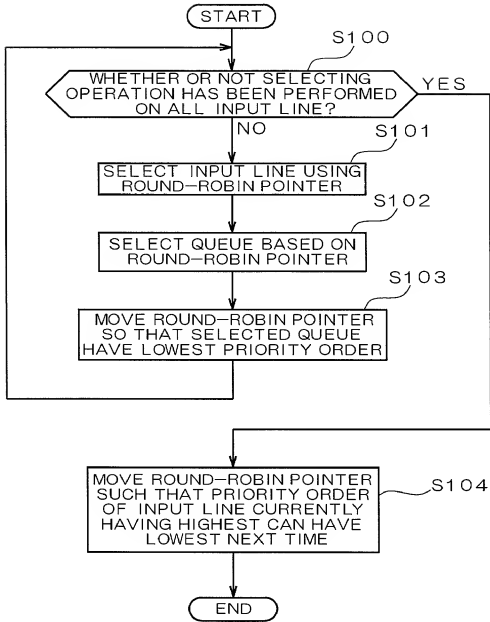


FIG. 5



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FIG. 6



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FIG. 7A

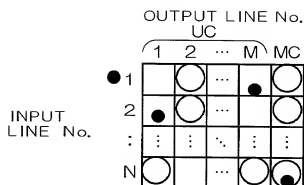


FIG. 7B

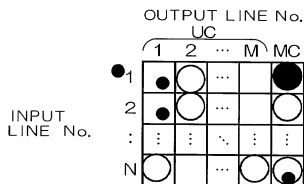


FIG. 7C

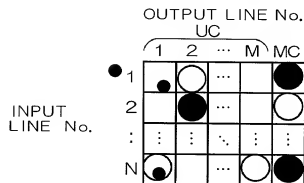


FIG. 7D

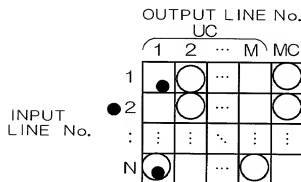


FIG. 8

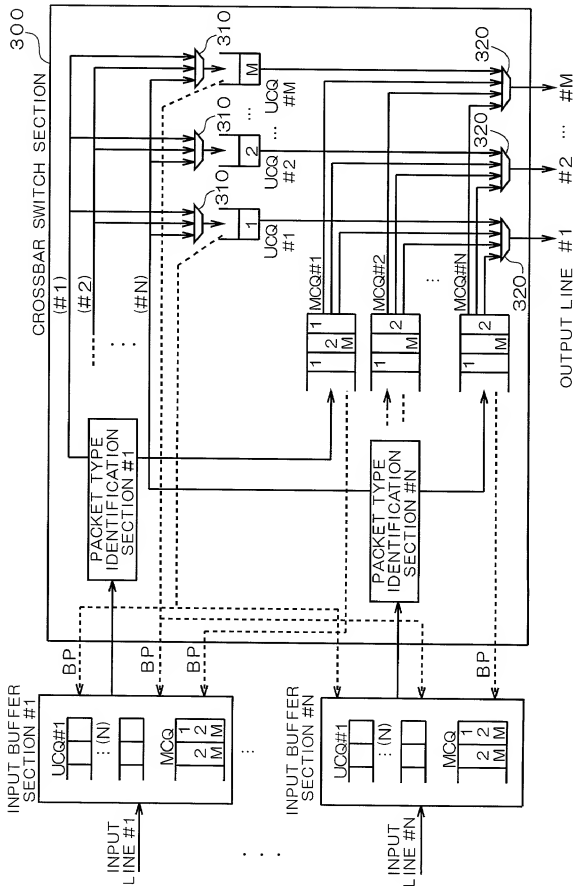
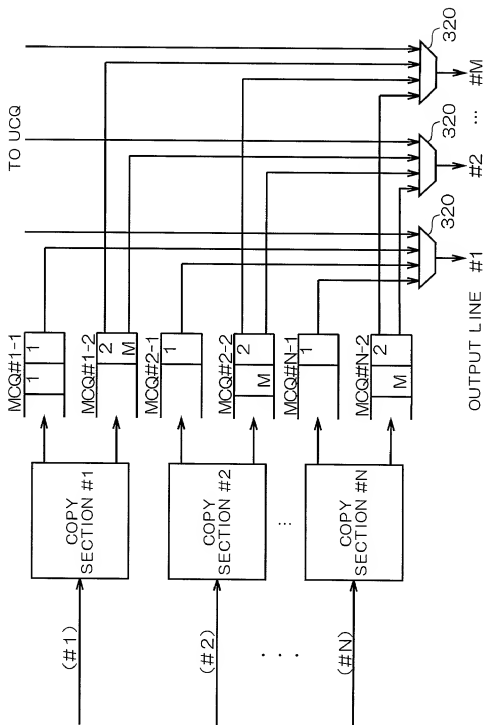


FIG. 9



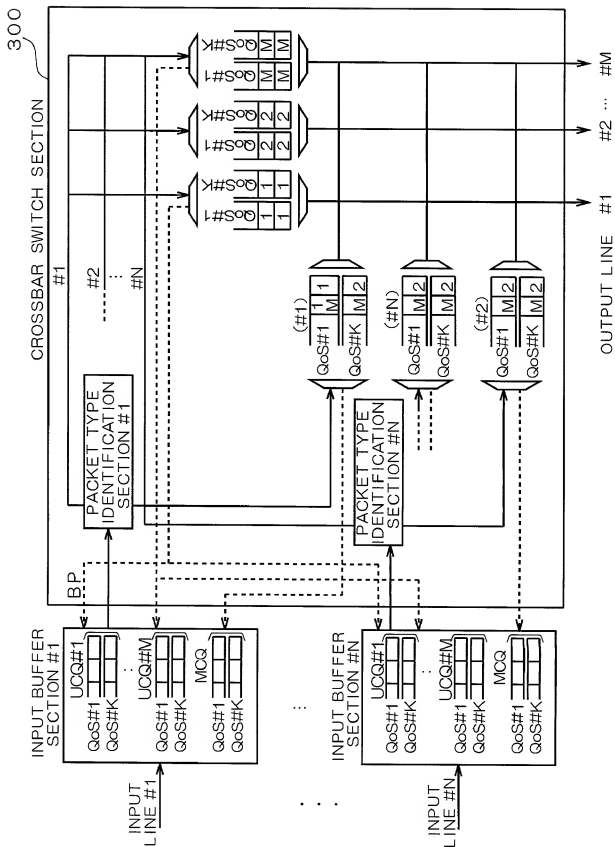


FIG. 11

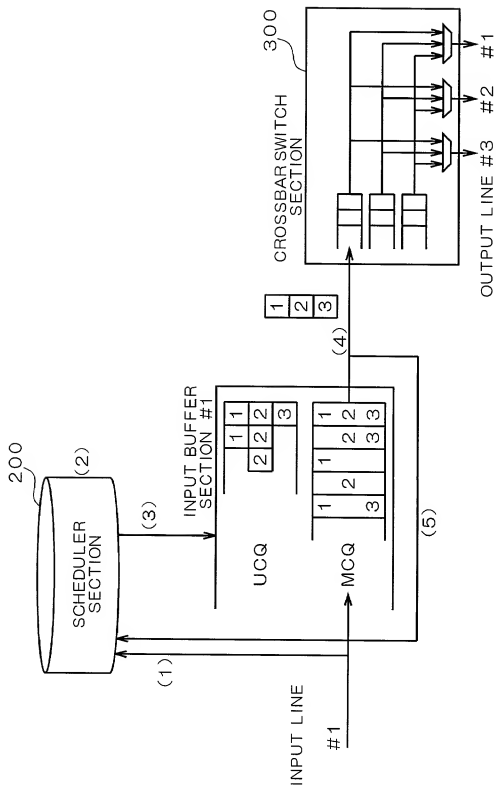


FIG. 12

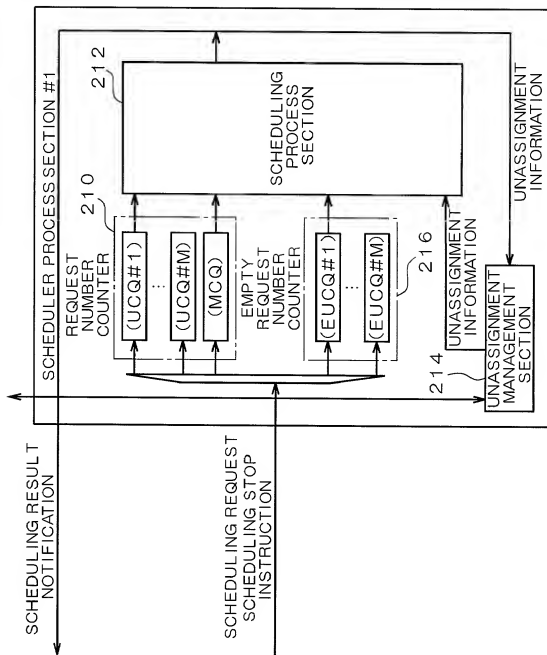
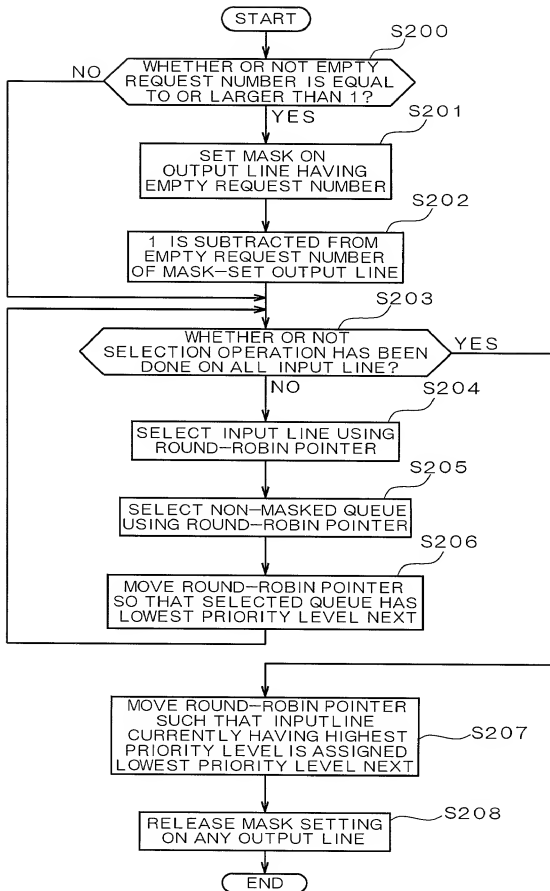


FIG. 13





OUTPUT LINE No.
UC



OUTPUT LINE No.
UC



OUTPUT LINE No.
UC



FIG. 15

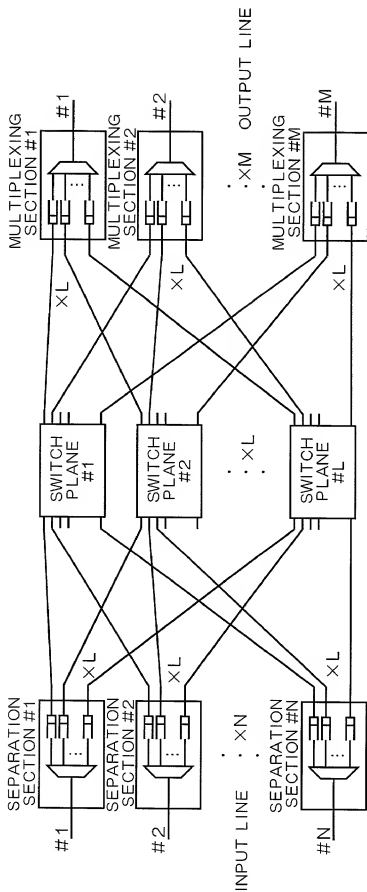


FIG. 16



FIG. 17

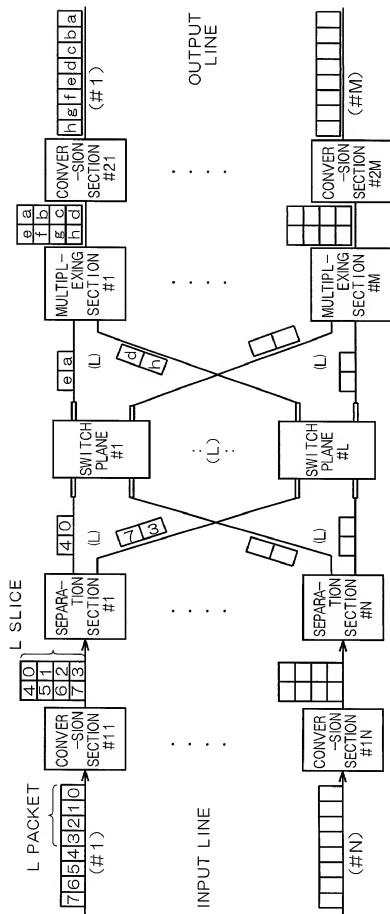


FIG. 18

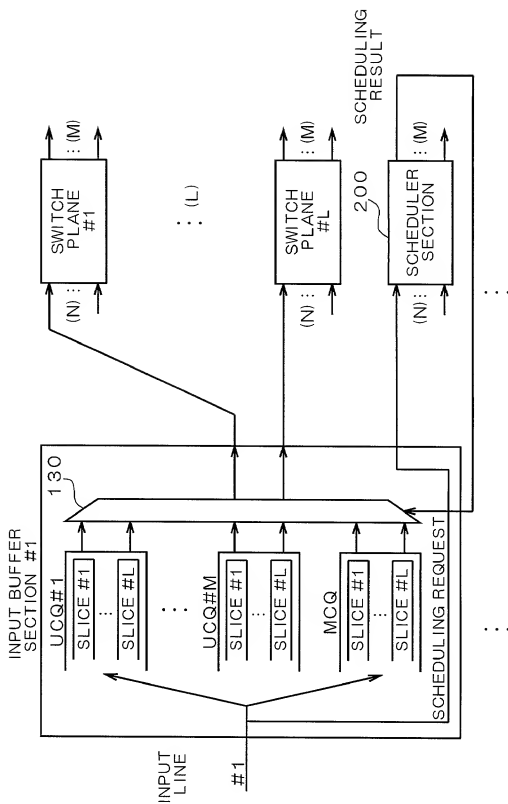


FIG. 20

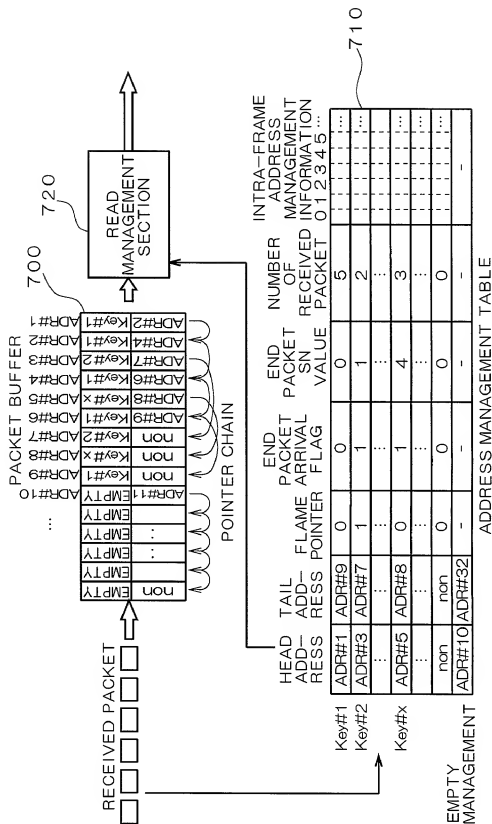
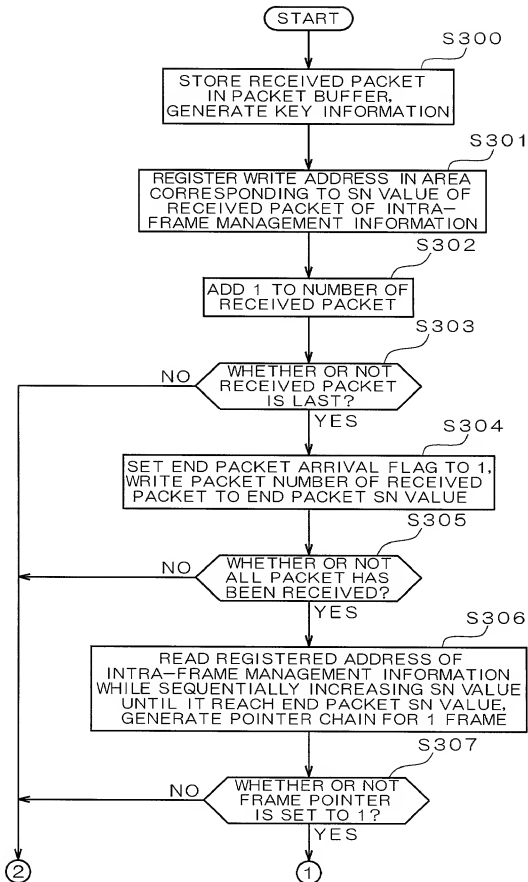
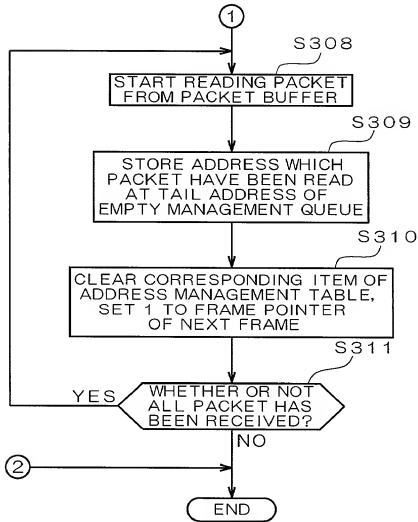


FIG. 21



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FIG. 22



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FIG. 23

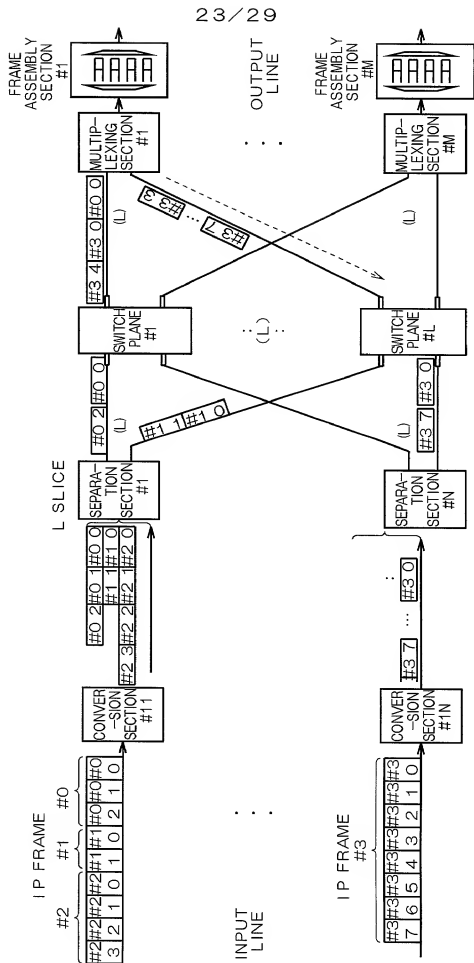
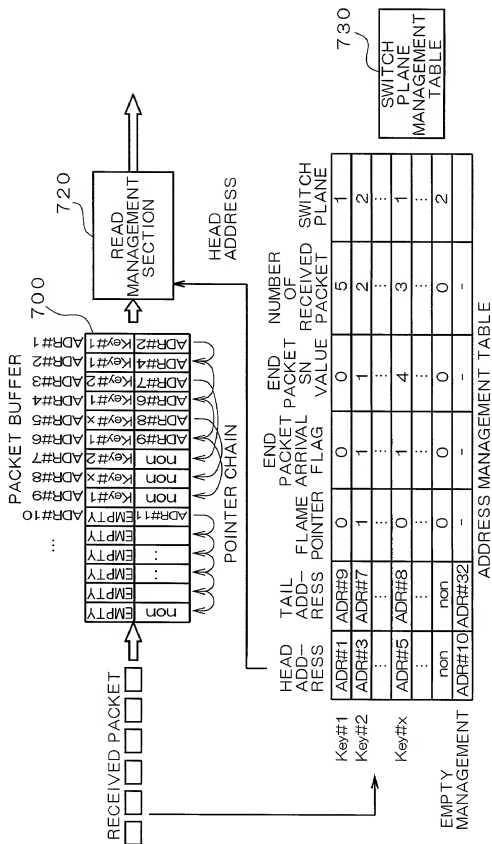
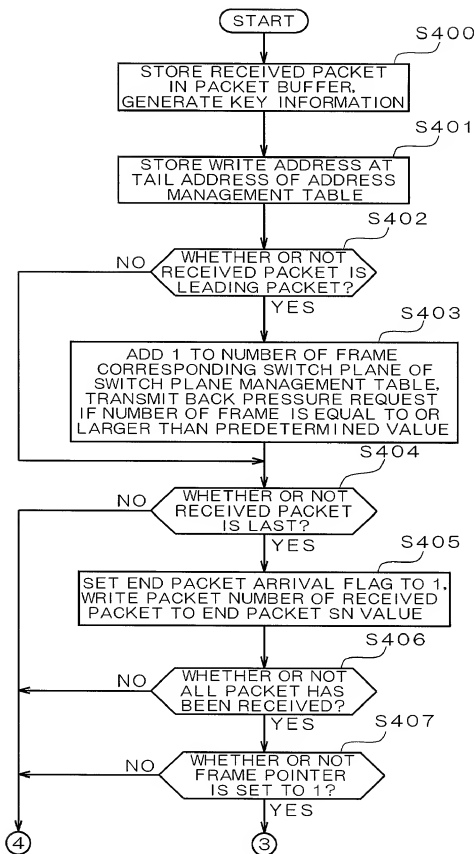


FIG. 24





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FIG. 26

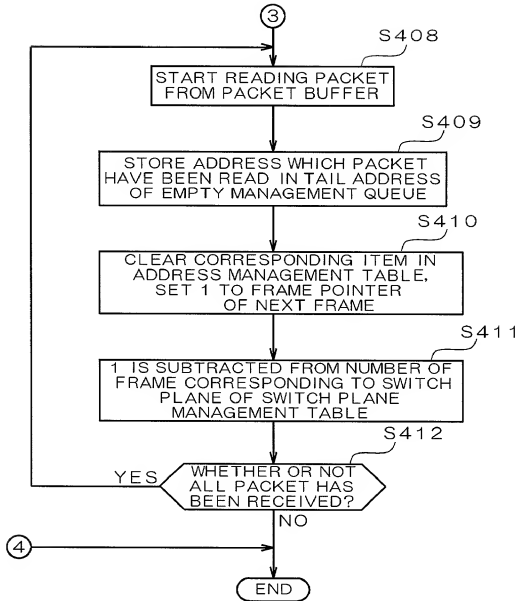


FIG. 27

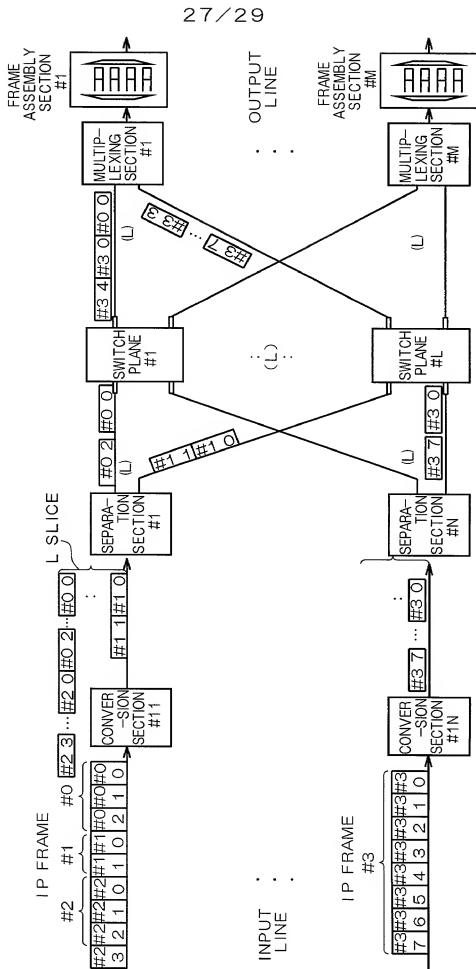


FIG. 28

PRIOR ART

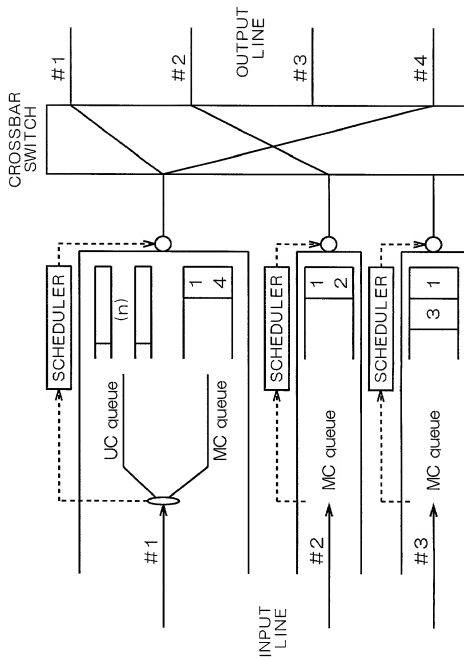


FIG. 29

PRIOR ART

